## CLAIMS

We claim:

1. A display controller for controlling a panel, comprising:

a display port capable of generating image data for display on the panel responsive to a display clock; and

a timing controller capable of generating start and clock pulses for driving the panel responsive to predetermined characteristics of the image data.

2. The display controller of claim 1 where the timing controller is capable of providing interlaced image data to the panel responsive to the start and clock pulses.

3. The display controller of claim 1 where the timing controller is capable of receiving synchronization signals from the display port.

4. The display controller of claim 1 where the clock pulse is pulsed at least twice for every vertical synchronization signal.

5. The display controller of claim 1 where the start pulse is capable of sequentially activating panel rows responsive to the clock pulse.

6. The display controller of claim 5 where the start pulse is capable of sequentially activating every other panel row responsive to the clock pulse.

7. The display controller of claim 1 where the predetermined characteristics include a vertical image frequency.

8. The display controller of claim 1 where the clock pulse increments a line counter such that the timing controller skips every other image line.

9. The display controller of claim 1 where timing controller comprises:

an output circuit capable of generating a function responsive to a top, bottom, left, and right position and a display clock;

a pulse width modulation circuit capable of generating a modulated pulse responsive to the display clock; and

a multiplexer circuit capable of selecting one of a plurality of inputs including the function responsive to the display clock.

10. The display controller of claim 9 where the output circuit comprises:

a plurality of set/reset flip flops capable of operating responsive to the display clock; and

a plurality of d-flip flops capable of operating responsive to flip flop outputs; and

a plurality of logic gates capable of logically manipulating the flip flop outputs.

11. The display controller of claim 9 where the output circuit is programmable.

12. The display controller of claim 9 where pulse width modulation circuit comprises a programmable counter capable of operating responsive to the display clock.

13. The display controller of claim 9 where the multiplexer circuit is capable of selecting between outputs generated by the output circuit.

14. The display controller of claim 1 where the display port and the timing controller are integrated in a single semiconductor device.

15. A controller for driving a flat panel, comprising:

means for generating display data capable of being displayed on the panel; and

means for timing the panel capable of generating control signals responsive to predetermined characteristics of the display data.

16. The controller of claim 15 comprising means for generating a display clock associated with the display data.

17. The controller of claim 15 comprising means for generating vertical and horizontal synchronization signals associated with the display data.

18. The controller of claim 15 where the means for generating display data is capable of generating deinterlaced display data.

19. The controller of claim 15 where the control signals includes vertical start and clock pulses for driving panel rows.

20. The controller of claim 19 where the means for timing the panel include means for generating at least two clock pulses for every vertical synchronization signal.

21. The controller of claim 20 comprising means for incrementing a line counter responsive to the clock pulses.

22. The controller of claim 20 where the means for timing include means for programming the vertical start pulse such that it activates alternating lines on alternating fields.

23. The controller of claim 15 where the means for timing every other line of data to the panel.

24. A timing controller, comprising:

a clock pulse circuit capable of generating a clock pulse responsive to a synchronization signal, the clock pulse having at least two pulses for every synchronization signal; and

a start pulse circuit capable of generating a start pulse responsive to the clock pulse.

25. The timing controller of claim 24 where the clock pulse is capable of skipping every other data line responsive to the clock pulse.

26. The timing controller of claim 24 where the clock pulse increments a line counter.

27. The timing controller of claim 24 where the start pulse sequentially drives panel rows responsive to the clock pulse.

28. The timing controller of claim 24 where the start pulse is programmed to occur coincident with a first line of a first field and with a second line of a second field.

29. A method, comprising:

generating display data capable of being displayed on flat panel; and

generating timing control signals for driving rows and columns of the flat panel responsive to predetermined characteristics of the display data.

30. The method of claim 29 comprising generating a synchronization signals associated with the display data.

31. The method of claim 29 where generating the timing control signals includes generating vertical start and clock pulses for driving the panel rows.

32. The method of claim 29 where generating the timing control signals includes generating at least two vertical clock pulses for each vertical synchronization signal.

33. The method of claim 32 where generating the timing control signals includes generating at least two vertical clock pulses responsive to a predetermined vertical frequency of the display data.

34. The method of claim 32 where generating the timing control signals includes incrementing a line counter with each vertical clock pulse.

35. The method of claim 29 where generating the timing control signals includes programming the vertical start pulse such that it activates alternating lines on alternating fields.